Amendment to the Claims:

A listing of the claims is provided below and will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

WE CLAIM:

Claim 1 (Currently amended): A memory control system, comprising:

a processor;

a bus in communication with the processor;

a first memory removed from said processor and in communication with the processor in a first data path removed from the bus; and

a second memory removed from said processor and in communication with the processor in a second data path removed from the bus and having an empty memory indicator;

wherein, in response to the second memory containing no application data, the second memory provides a corresponding indication to the processor.

Claim 2 (Original): The system of claim 1, further comprising:

a hub in communication with the bus to provide application data to the processor.

Claim 3 (Currently amended) A memory control system, comprising:

a controller module having a first data path, a second data path, and a bus; and

a first memory in communication with the first data path; and

a second memory in communication with the second data path and having an empty memory indicator;

wherein the controller module replicates data from the first memory to the second memory in response to an empty data indication from the second memory.

Claim 4 (Original): The system of claim 3, further comprising:

an application module in communication with the controller module, wherein the controller module is connected to retrieve application data from the application module for storage in the first memory.

Claim 5 (Original): The system of claim 3, further comprising:

a memory module in communication with the controller module and containing the first memory and the second memory.

Claim 6 (Original): The system of claim 3, further comprising:

an application electrical connector on the application module; and

a controller electrical connector on the electrical applications controller in communication with the application electrical connector;

wherein each of said electrical connectors are axially symmetric to enable different relative rotational positions between the application and connector modules.

Claim 7 (Original): The system of claim 4, further comprising:

means for releasably connecting the application module to the electrical applications controller, said means enabling the application module and the electrical applications controller to be disengaged and break electrical communication between them, rotated 180 degrees and reengaged to reestablish electrical communication between them.

Claim 8 (Currently amended): A method of installing a new memory that has a ~~predetermined~~ predetermined memory capacity into a system that comprises a processor and first old memory, with the first old memory storing an amount of application data to produce a redundant array of independent memories, comprising:

initiating a duplication function in the processor;

transmitting an empty data indication from the new memory to the processor; and

replicating the application data from the first old memory to the new memory.

Claim 9 (Original): The method of claim 8, wherein replicating the application data comprises comparing the amount of application data in the first old memory to the capacity of the new memory to determine whether said capacity is sufficient to hold the application data.

Claims 10-11 (Cancelled)

Claim 12 (Currently amended): ~~The method of claim 11,~~ A method of installing a new memory that has a predetermined capacity and a new memory ID into a system that comprises a processor and first and second old memories having respective first and second memory IDs, said memories capable of storing application data, comprising:

removing the first old memory from the system;

installing the new memory into the system;

determining whether the new memory ID matches either of the first or second memory IDs; and

replicating the application data from the second old memory to the new memory if the new memory ID does not match either of the first or second memory IDs, to maintain a redundant array of independent memories;

wherein said new memory transmits an empty data indication to said processor if said new memory does not store any data, and said transmission enables said data replication.